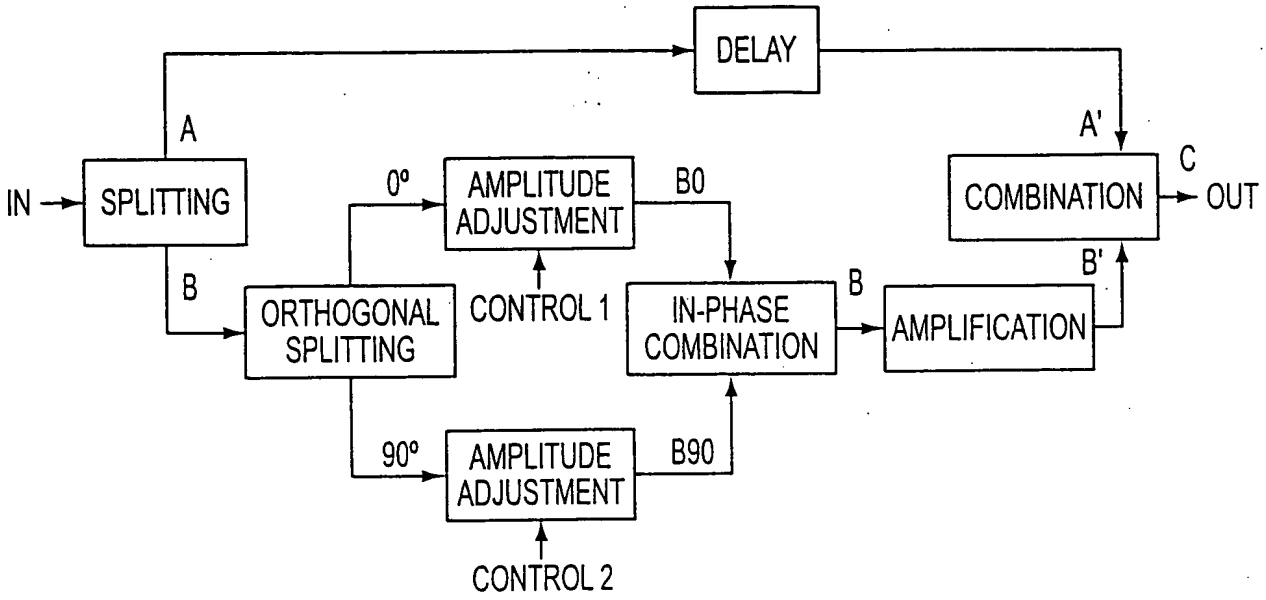
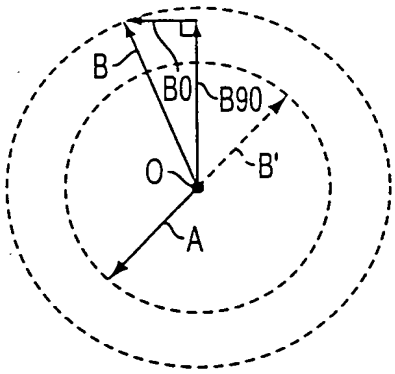
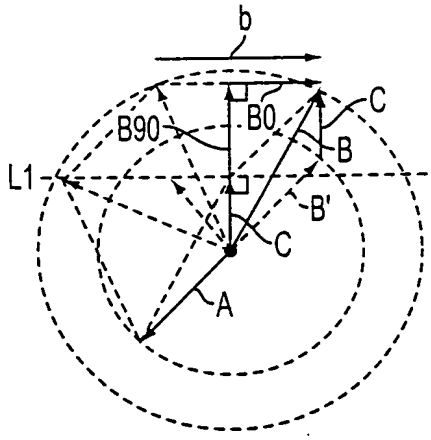


FIG. 1A



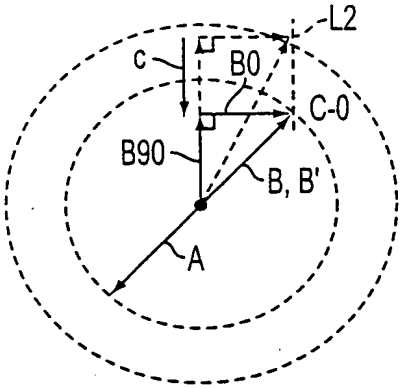
INITIAL STATUS

FIG. 1B



B0 AMPLITUDE CONTROL

FIG. 1C



B90 AMPLITUDE CONTROL

FIG. 1D

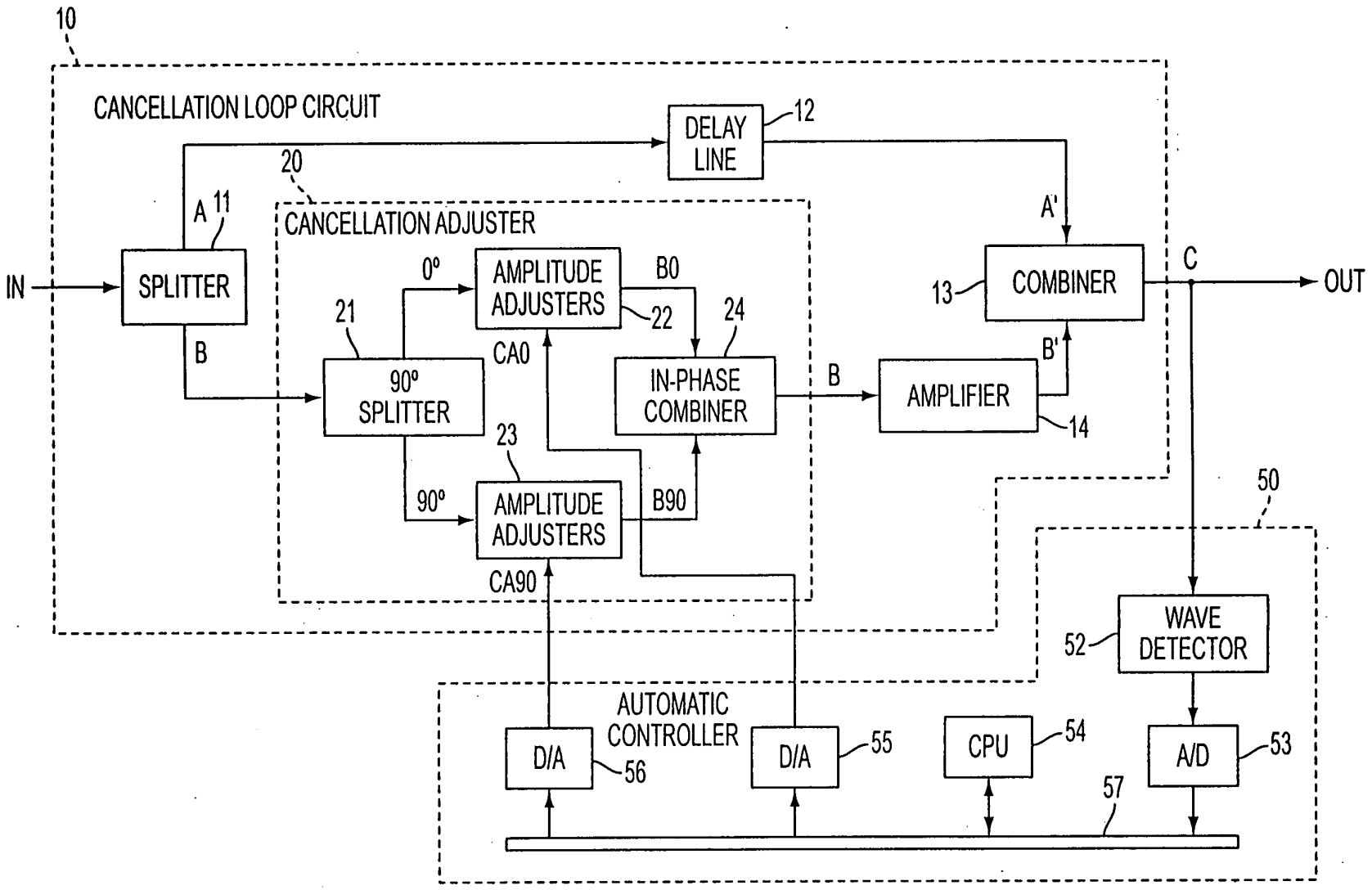
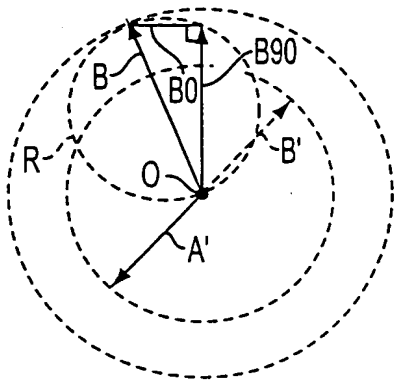
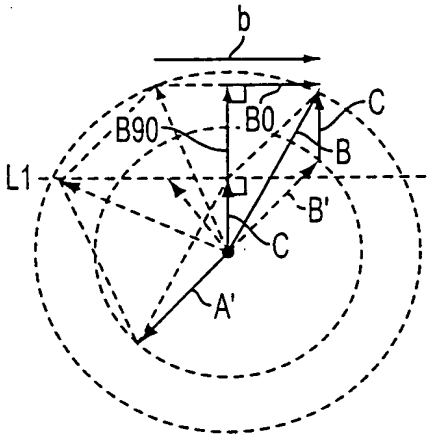

10
CANCELLATION LOOP CIRCUIT
DELAY LINE
12
20
CANCELLATION ADJUSTER
A
11
A'
IN
SPLITTER
0°
AMPLITUDE ADJUSTERS
B0
22
24
C
OUT
13
COMBINER
21
B
CA0
90° SPLITTER
IN-PHASE COMBINER
B
AMPLIFIER
B'
14
23
90°
AMPLITUDE ADJUSTERS
B90
50
CA90
WAVE DETECTOR
52
AUTOMATIC CONTROLLER
D/A
56
D/A
55
CPU
54
A/D
53
57

FIG. 2



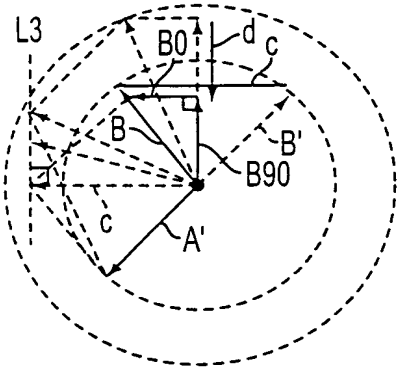
INITIAL STATUS

FIG. 3A



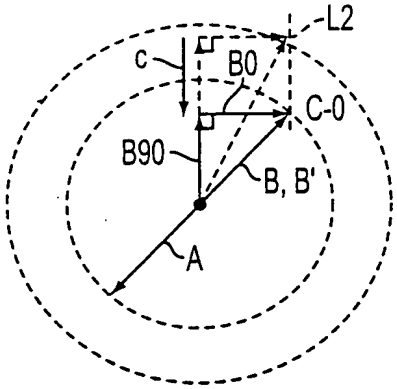
B0 AMPLITUDE CONTROL

FIG. 3B



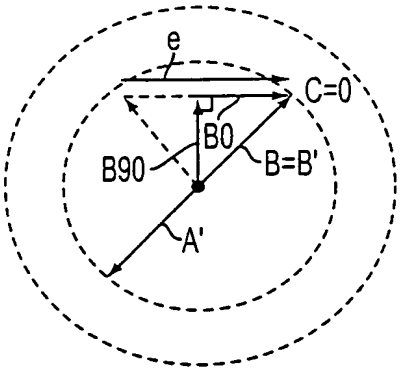
B90 AMPLITUDE CONTROL

FIG. 3D



B90 AMPLITUDE CONTROL

FIG. 3C



B0 AMPLITUDE CONTROL

FIG. 3E

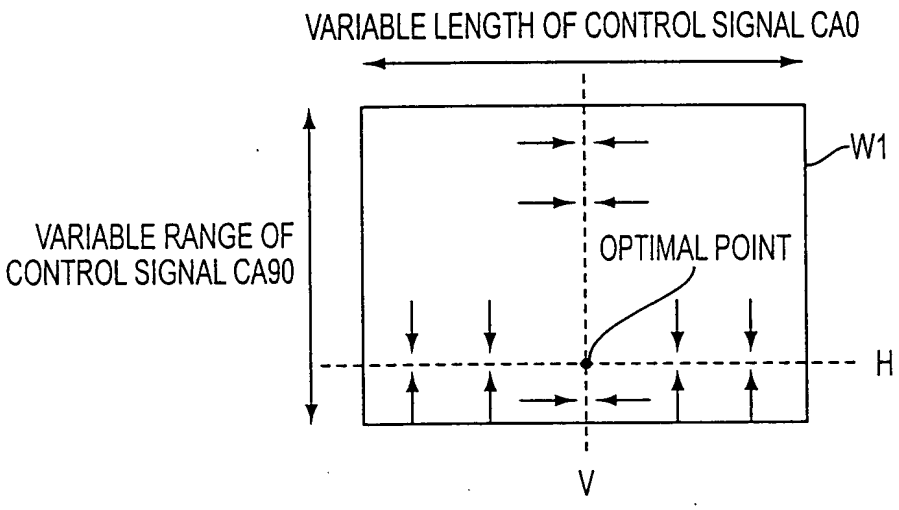

VARIABLE LENGTH OF CONTROL SIGNAL CA0
W1
VARIABLE RANGE OF
CONTROL SIGNAL CA90
OPTIMAL POINT
H
V

FIG. 4

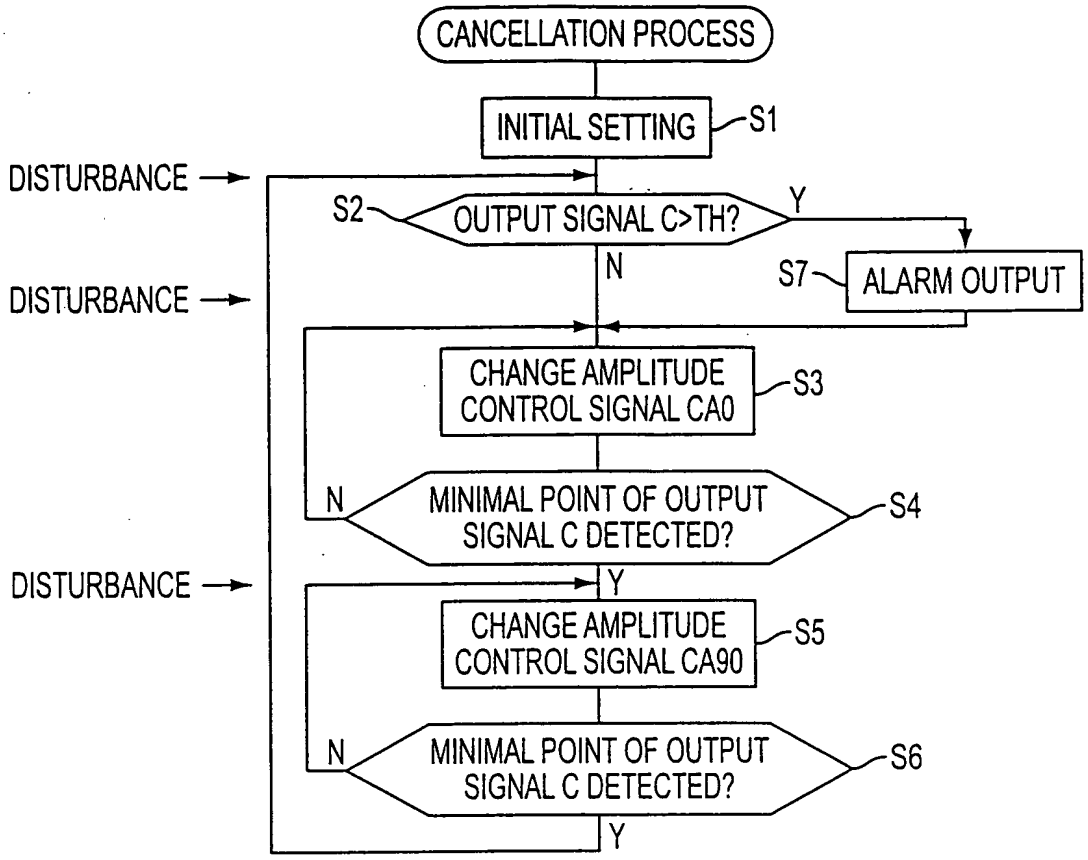

CANCELLATION PROCESS
INITIAL SETTING
S1
DISTURBANCE
S2
OUTPUT SIGNAL C>TH?
Y
N
S7
ALARM OUTPUT
DISTURBANCE
CHANGE AMPLITUDE CONTROL SIGNAL CA0
S3
N
MINIMAL POINT OF OUTPUT SIGNAL C DETECTED?
S4
DISTURBANCE
Y
CHANGE AMPLITUDE CONTROL SIGNAL CA90
S5
N
MINIMAL POINT OF OUTPUT SIGNAL C DETECTED?
S6
Y

FIG. 5A

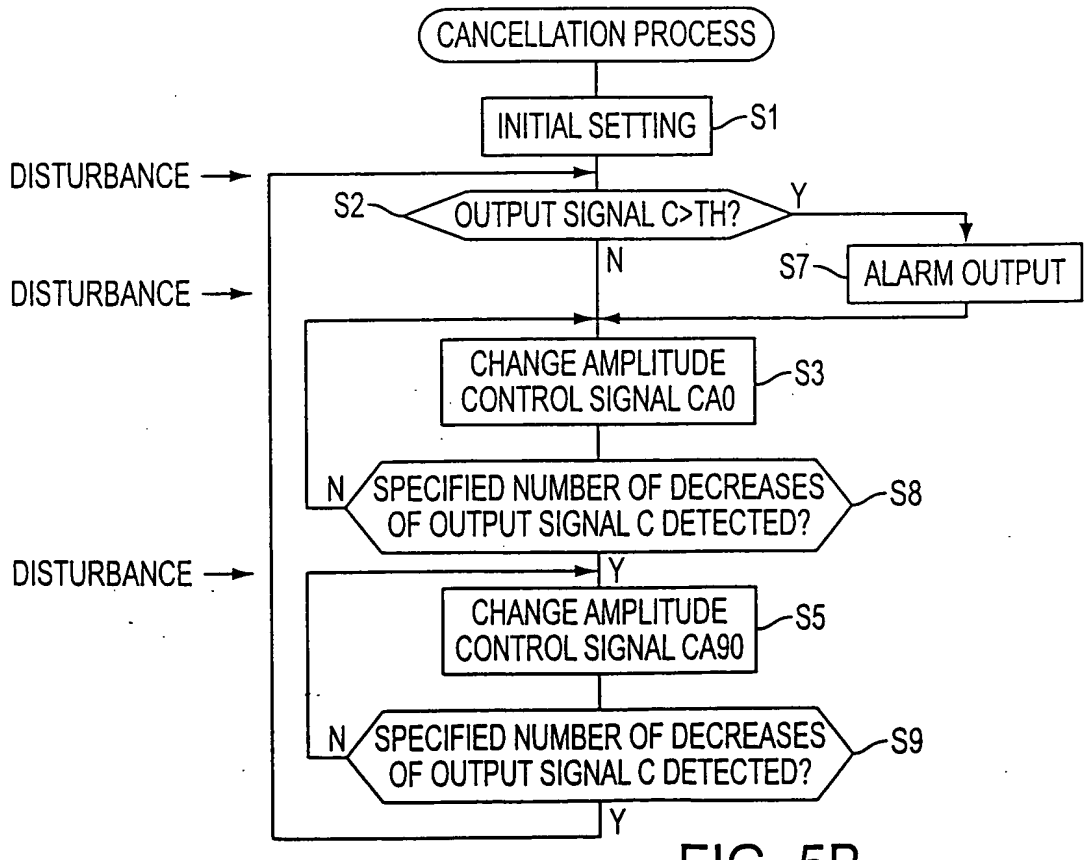

CANCELLATION PROCESS
INITIAL SETTING
S1
DISTURBANCE
S2
OUTPUT SIGNAL C>TH?
Y
N
S7
ALARM OUTPUT
DISTURBANCE
CHANGE AMPLITUDE CONTROL SIGNAL CA0
S3
N
SPECIFIED NUMBER OF DECREASES OF OUTPUT SIGNAL C DETECTED?
S8
DISTURBANCE
Y
CHANGE AMPLITUDE CONTROL SIGNAL CA90
S5
N
SPECIFIED NUMBER OF DECREASES OF OUTPUT SIGNAL C DETECTED?
S9
Y

FIG. 5B

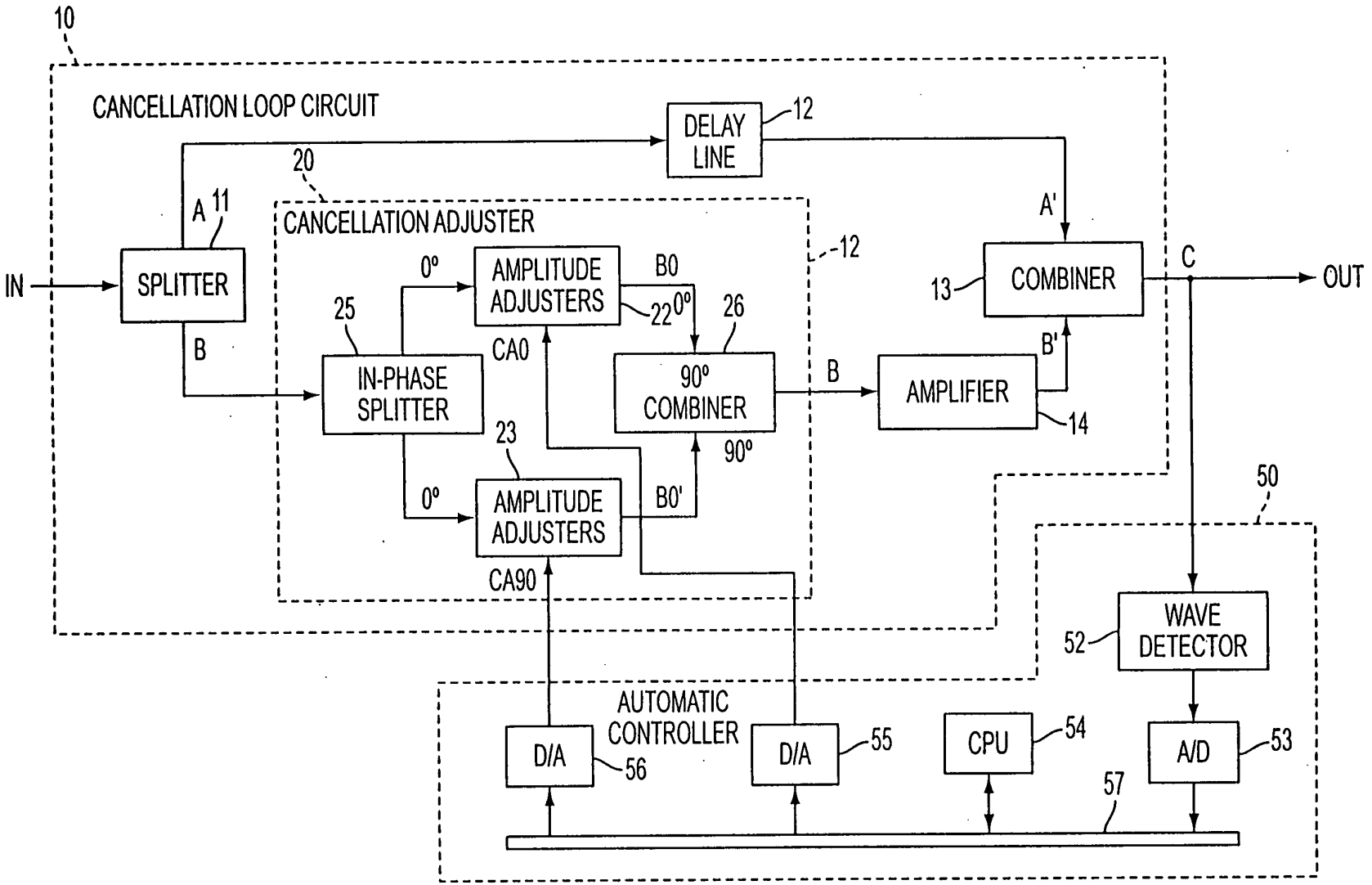

10
CANCELLATION LOOP CIRCUIT
DELAY LINE
12
20
A
11
CANCELLATION ADJUSTER
A'
12
IN
SPLITTER
0°
AMPLITUDE ADJUSTERS
B0
22
0°
26
C
OUT
13
COMBINER
25
B
CA0
IN-PHASE SPLITTER
90° COMBINER
B
AMPLIFIER
B'
14
90°
23
0°
AMPLITUDE ADJUSTERS
B0'
50
CA90
WAVE DETECTOR
52
AUTOMATIC CONTROLLER
D/A
56
D/A
55
CPU
54
A/D
53
57

FIG. 6

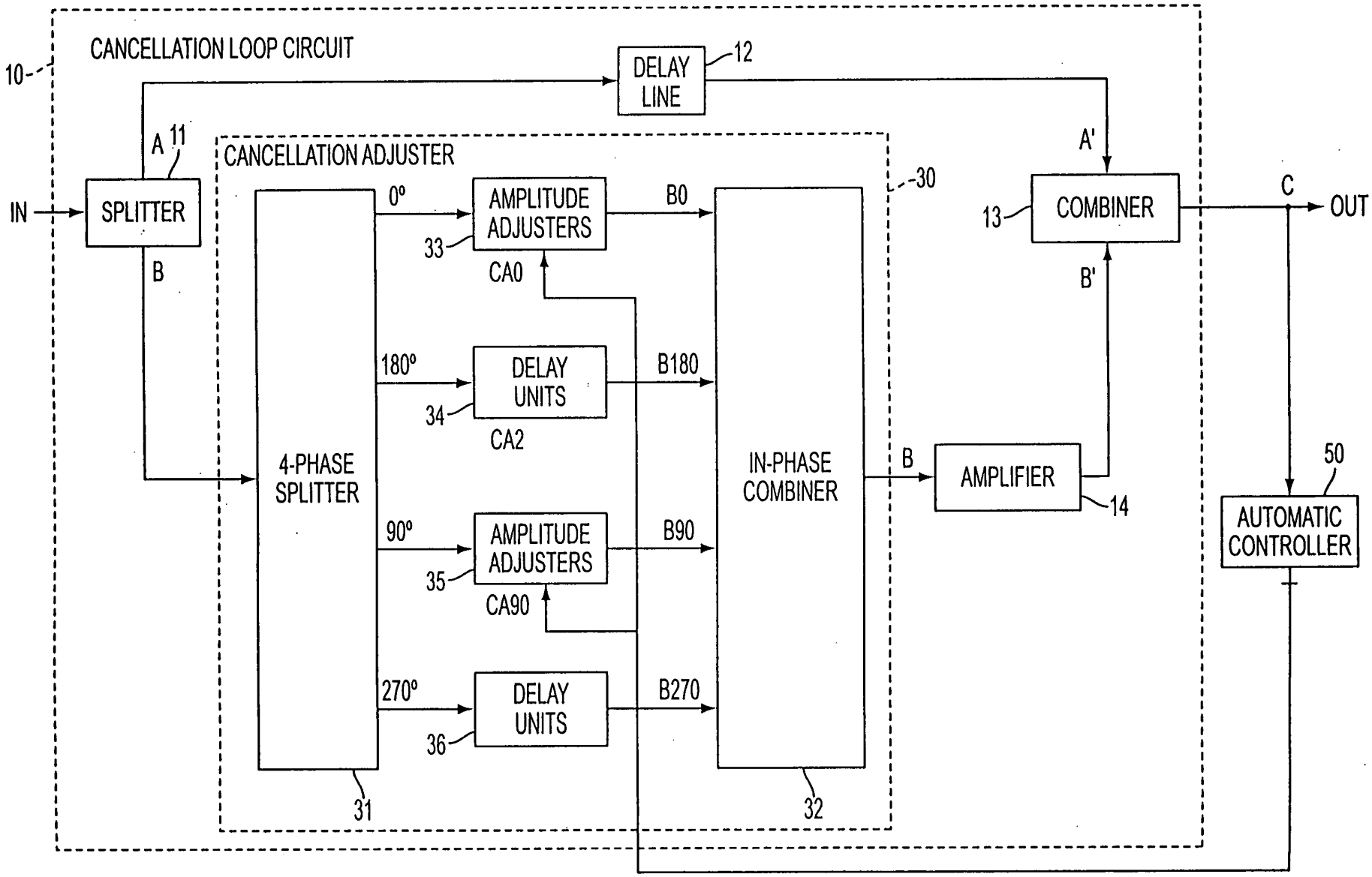

CANCELLATION LOOP CIRCUIT
10
DELAY LINE
12
A
11
CANCELLATION ADJUSTER
30
A'
IN
SPLITTER
B
0°
AMPLITUDE ADJUSTERS
33
CA0
B0
COMBINER
13
C
OUT
B'
180°
DELAY UNITS
34
CA2
B180
4-PHASE SPLITTER
IN-PHASE COMBINER
B
AMPLIFIER
14
50
AUTOMATIC CONTROLLER
90°
AMPLITUDE ADJUSTERS
35
CA90
B90
270°
DELAY UNITS
36
B270
31
32

FIG. 7

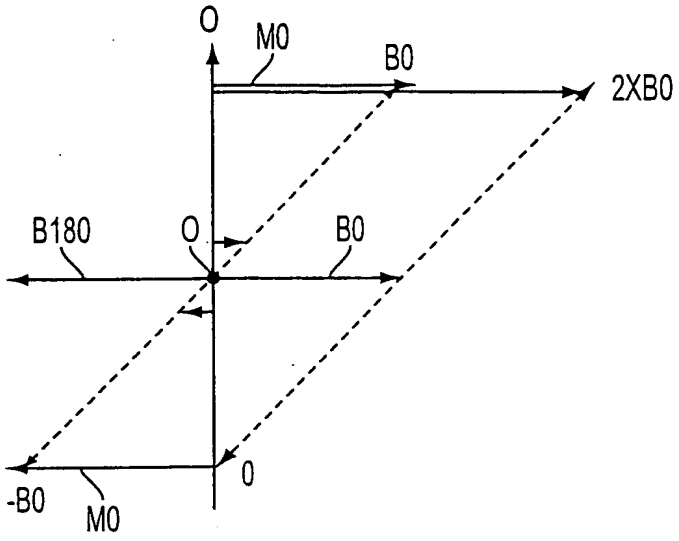


FIG. 8A

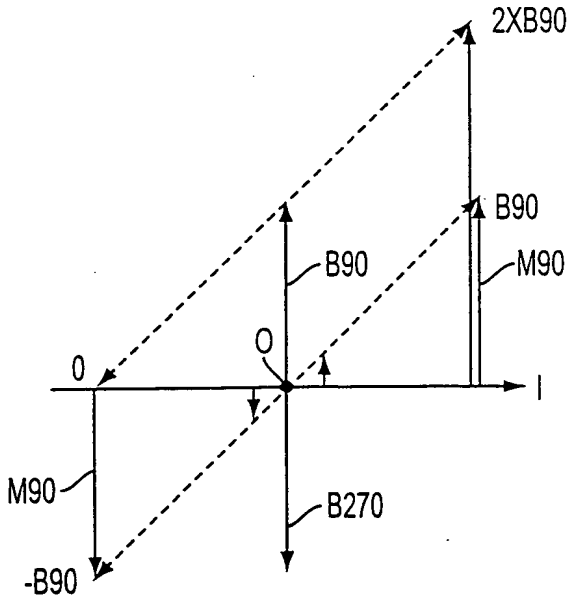


FIG. 8B

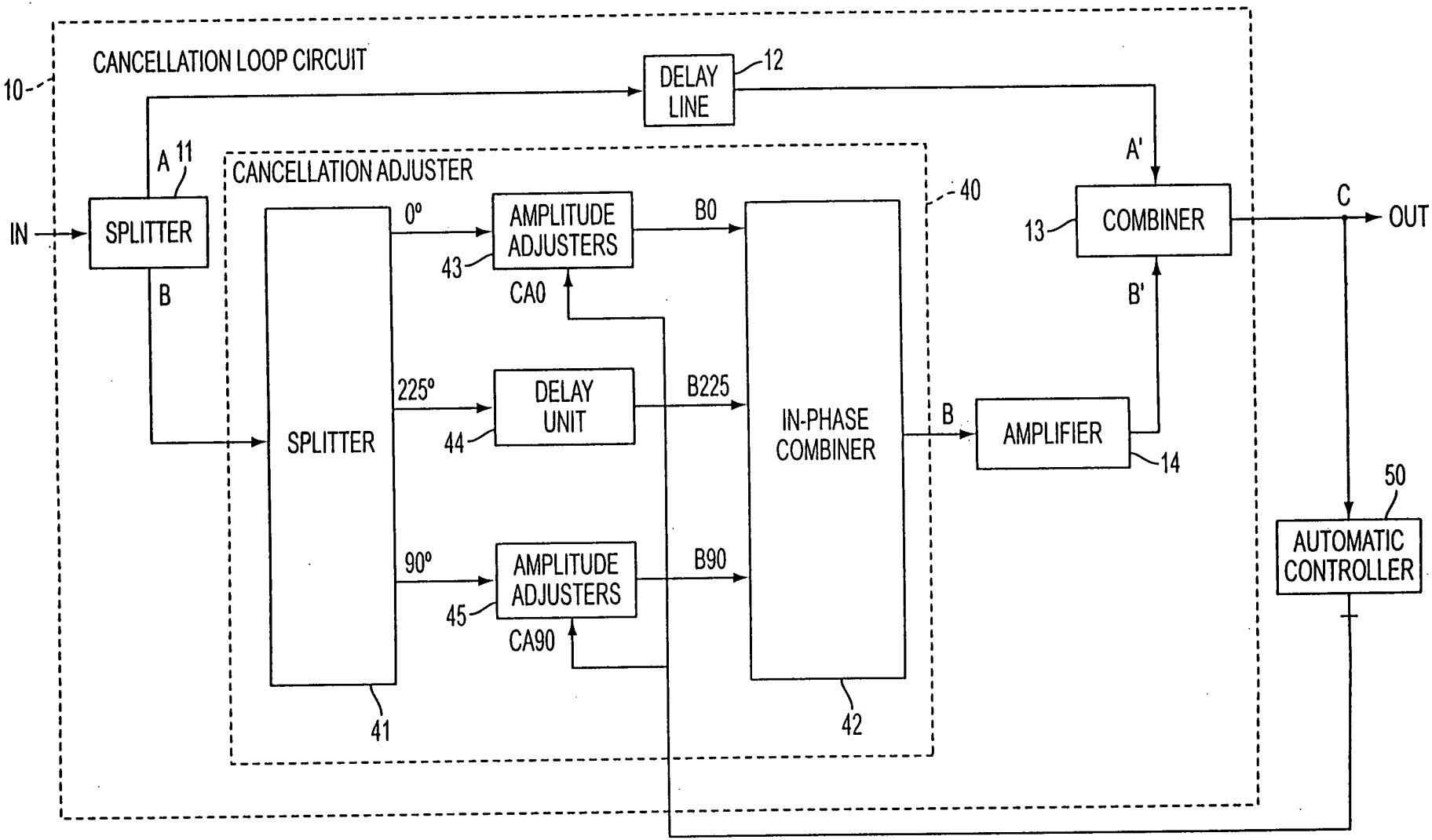

CANCELLATION LOOP CIRCUIT
10
DELAY LINE
12
A
11
A'
CANCELLATION ADJUSTER
40
IN
SPLITTER
B
0°
AMPLITUDE ADJUSTERS
43
CA0
B0
13
COMBINER
C
OUT
B'
SPLITTER
225°
DELAY UNIT
44
B225
IN-PHASE COMBINER
B
AMPLIFIER
14
50
AUTOMATIC CONTROLLER
90°
AMPLITUDE ADJUSTERS
45
CA90
B90
41
42

FIG. 9

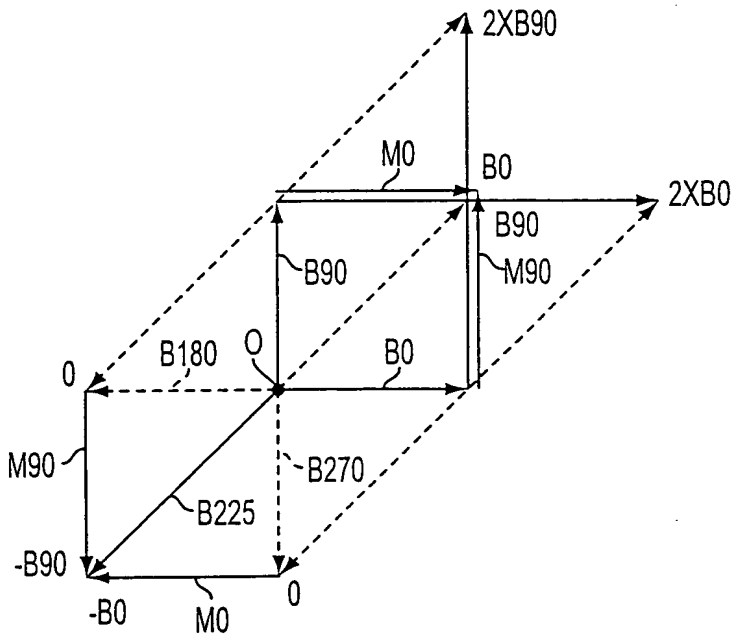


FIG. 10

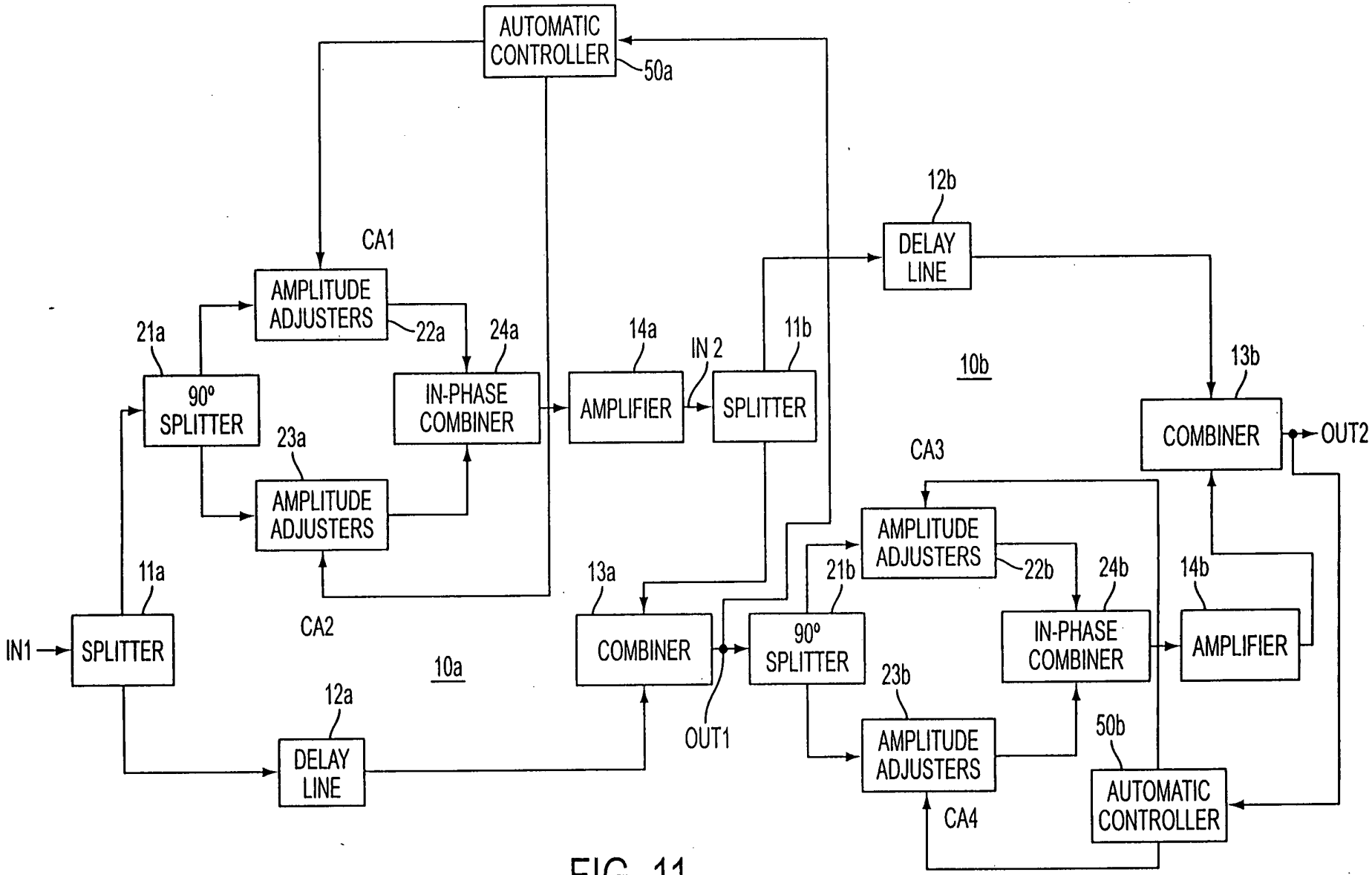

AUTOMATIC CONTROLLER
50a
CA1
AMPLITUDE ADJUSTERS
22a
24a
21a
90° SPLITTER
IN-PHASE COMBINER
14a
IN 2
AMPLIFIER
11b
SPLITTER
12b
DELAY LINE
10b
13b
COMBINER
OUT2
CA3
AMPLITUDE ADJUSTERS
22b
24b
14b
IN-PHASE COMBINER
AMPLIFIER
23a
AMPLITUDE ADJUSTERS
11a
IN1
SPLITTER
CA2
10a
13a
COMBINER
21b
90° SPLITTER
OUT1
23b
AMPLITUDE ADJUSTERS
50b
AUTOMATIC CONTROLLER
CA4
12a
DELAY LINE

FIG. 11

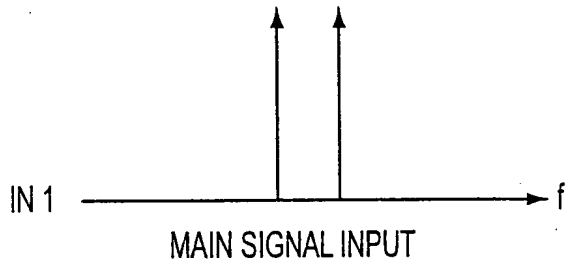


FIG. 12A

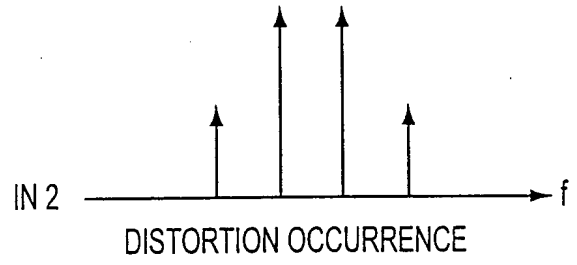


FIG. 12B

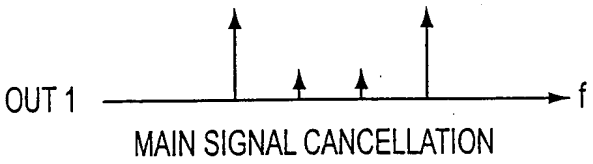


FIG. 12C

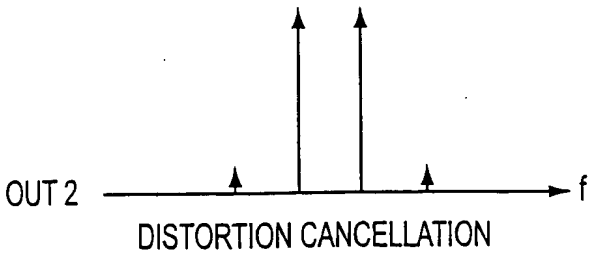
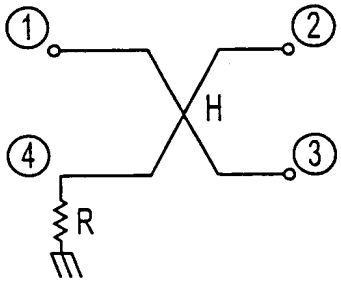
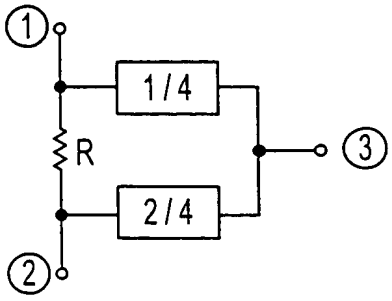


FIG. 12D



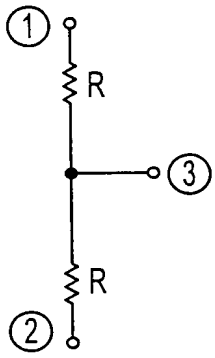
90° SPLITTER-COMBINER

FIG. 13A



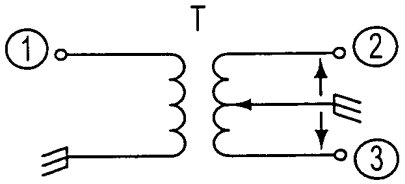
IN-PHASE SPLITTER-COMBINER

FIG. 13B



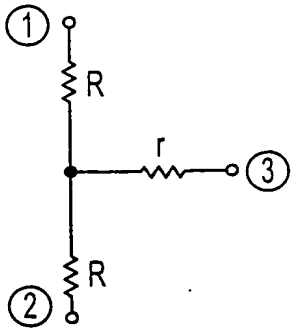
IN-PHASE SPLITTER-COMBINER

FIG. 13C



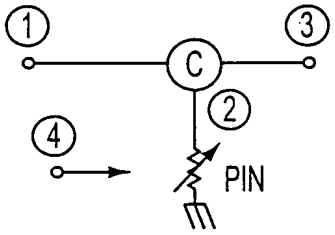
180° SPLITTER-COMBINER

FIG. 13D



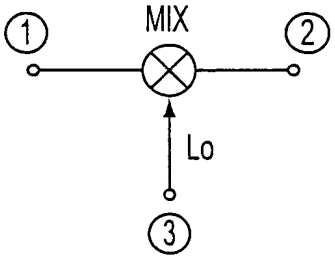
IN-PHASE SPLITTER-COMBINER

FIG. 13E



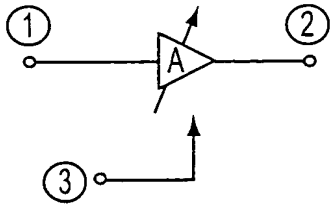
CIRCULATOR TYPE

FIG. 14A



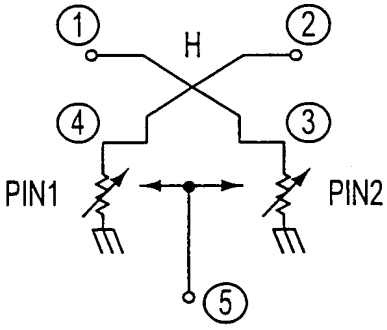
MIXER TYPE

FIG. 14B



GAIN CONTROL TYPE

FIG. 14C



HYBRID TYPE

FIG. 14D

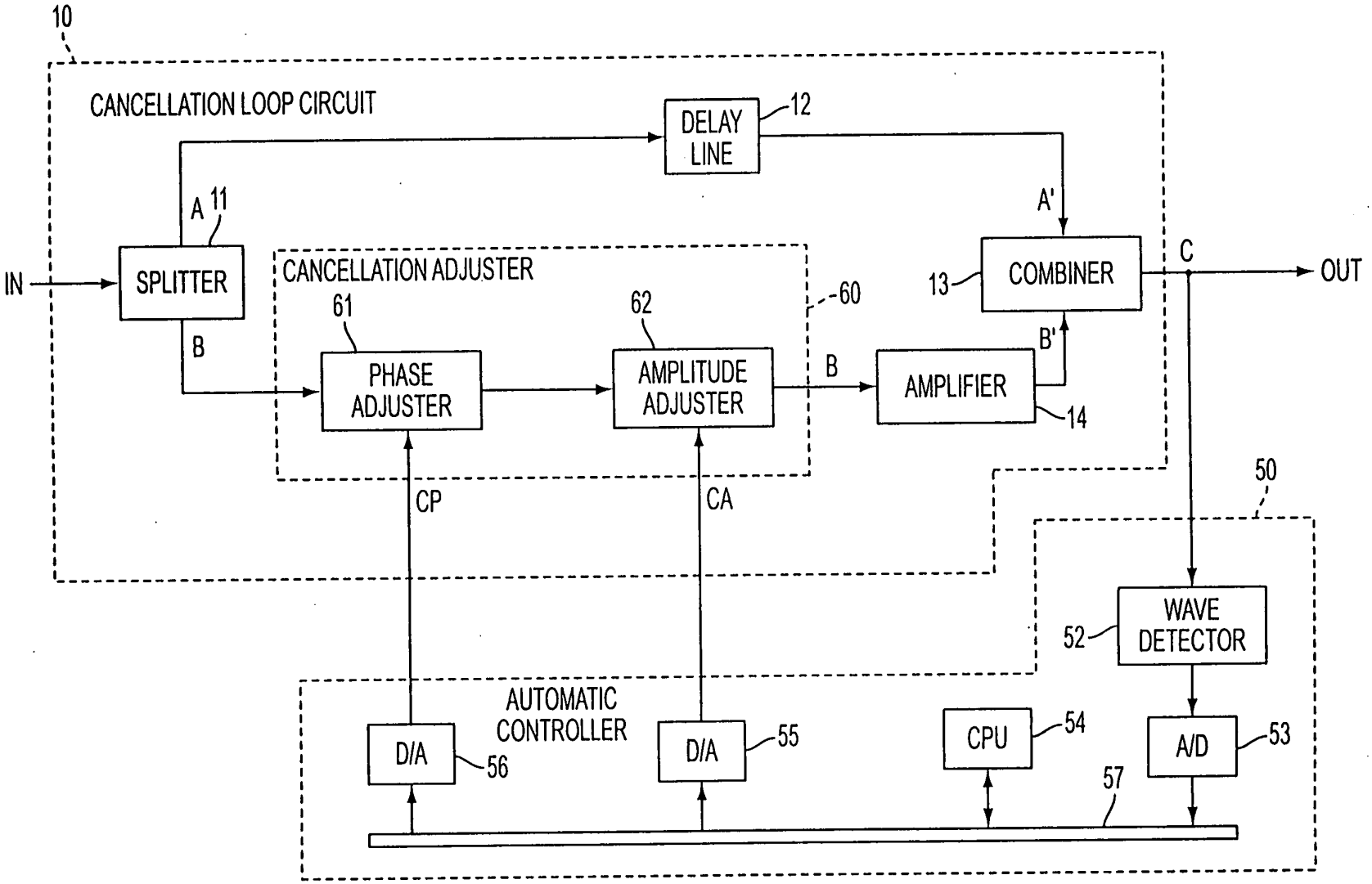
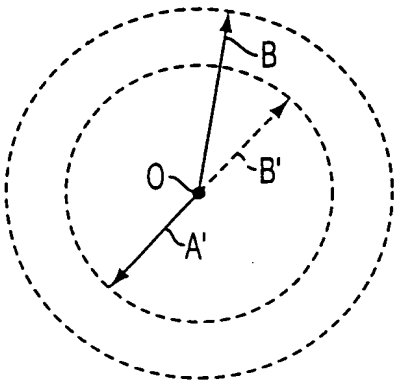
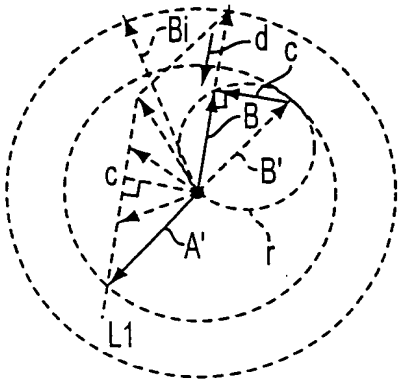

10
CANCELLATION LOOP CIRCUIT
DELAY LINE
12
A
11
A'
IN
SPLITTER
CANCELLATION ADJUSTER
60
13
COMBINER
C
OUT
61
62
B
PHASE ADJUSTER
AMPLITUDE ADJUSTER
B
AMPLIFIER
B'
14
CP
CA
50
WAVE DETECTOR
52
AUTOMATIC CONTROLLER
D/A
56
D/A
55
CPU
54
A/D
53
57

FIG. 15



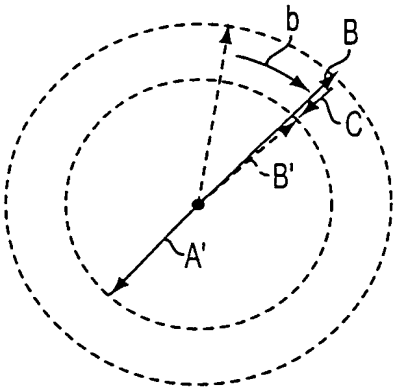
INITIAL STATUS

FIG. 16A



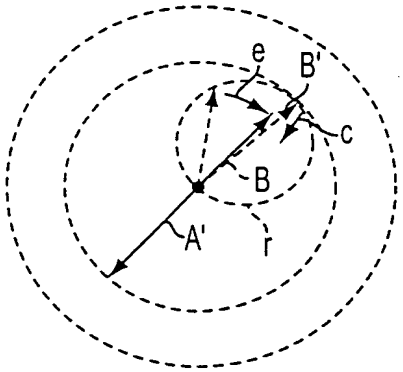
AMPLITUDE CONTROL

FIG. 16D



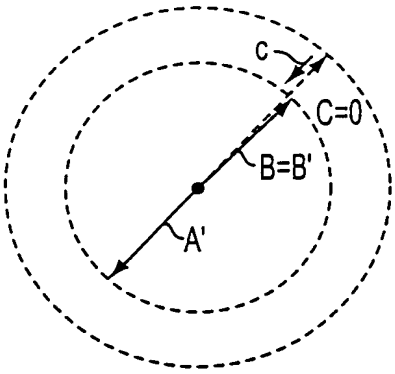
PHASE CONTROL

FIG. 16B



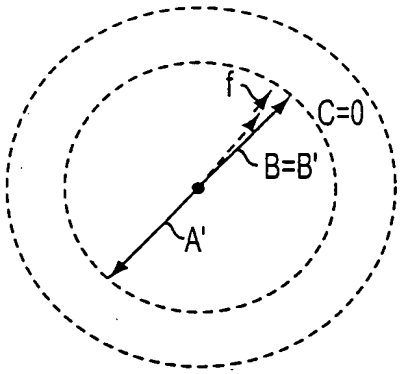
PHASE CONTROL

FIG. 16E



AMPLITUDE CONTROL

FIG. 16C



AMPLITUDE CONTROL

FIG. 16F

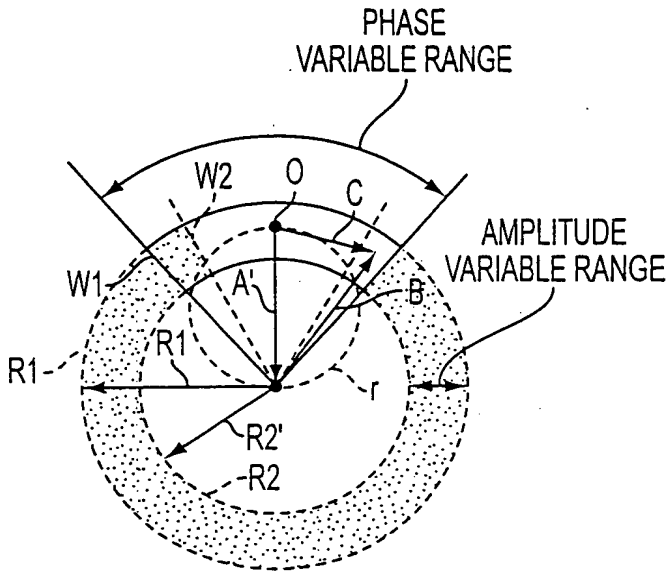


FIG. 17A

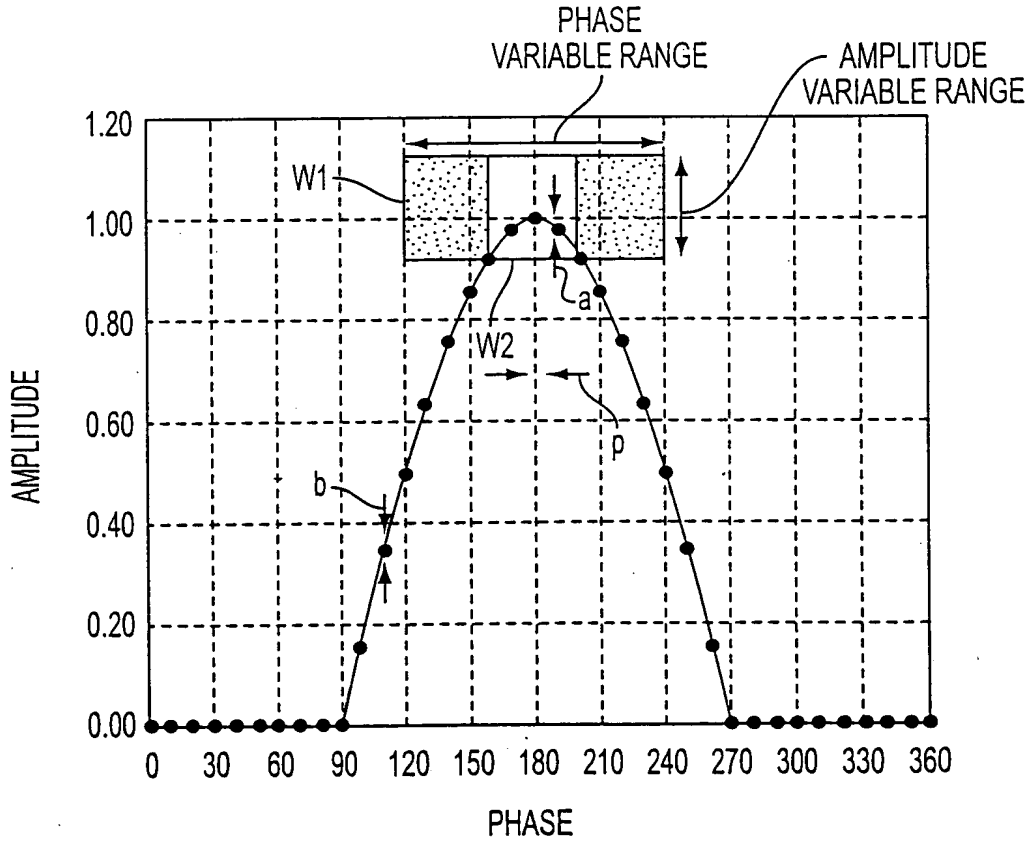


FIG. 17B

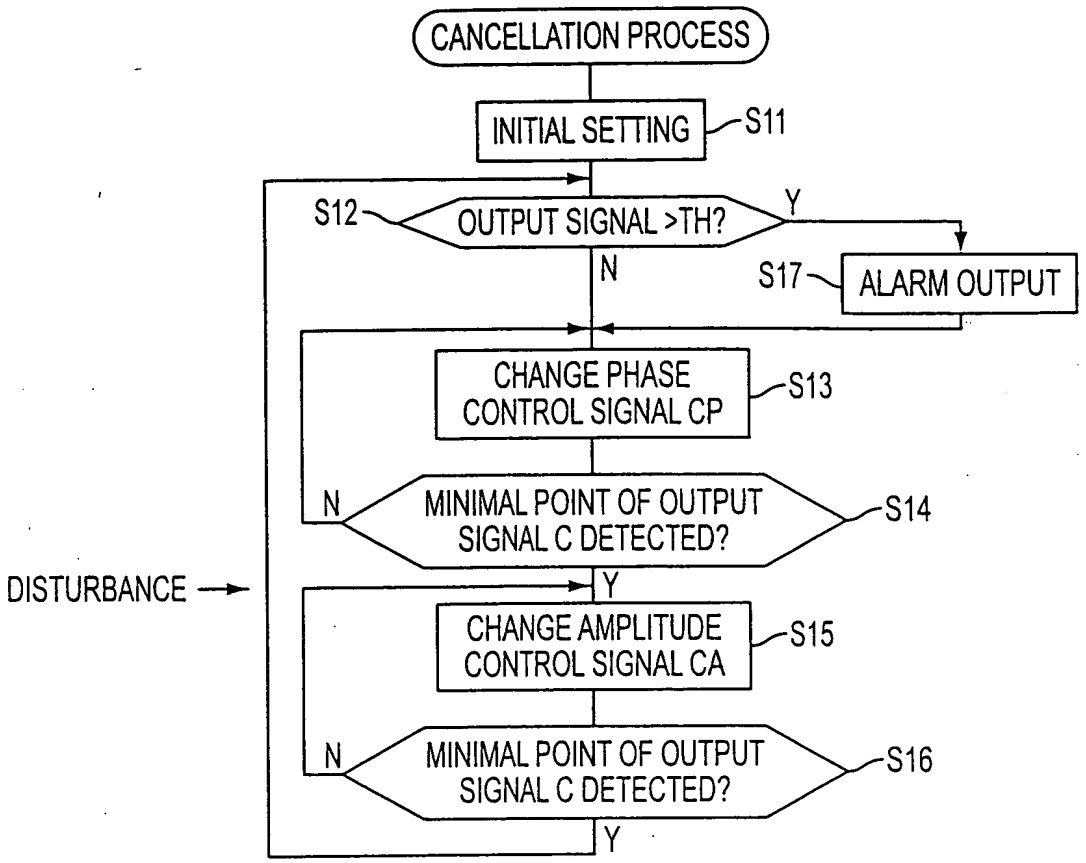


FIG. 18A

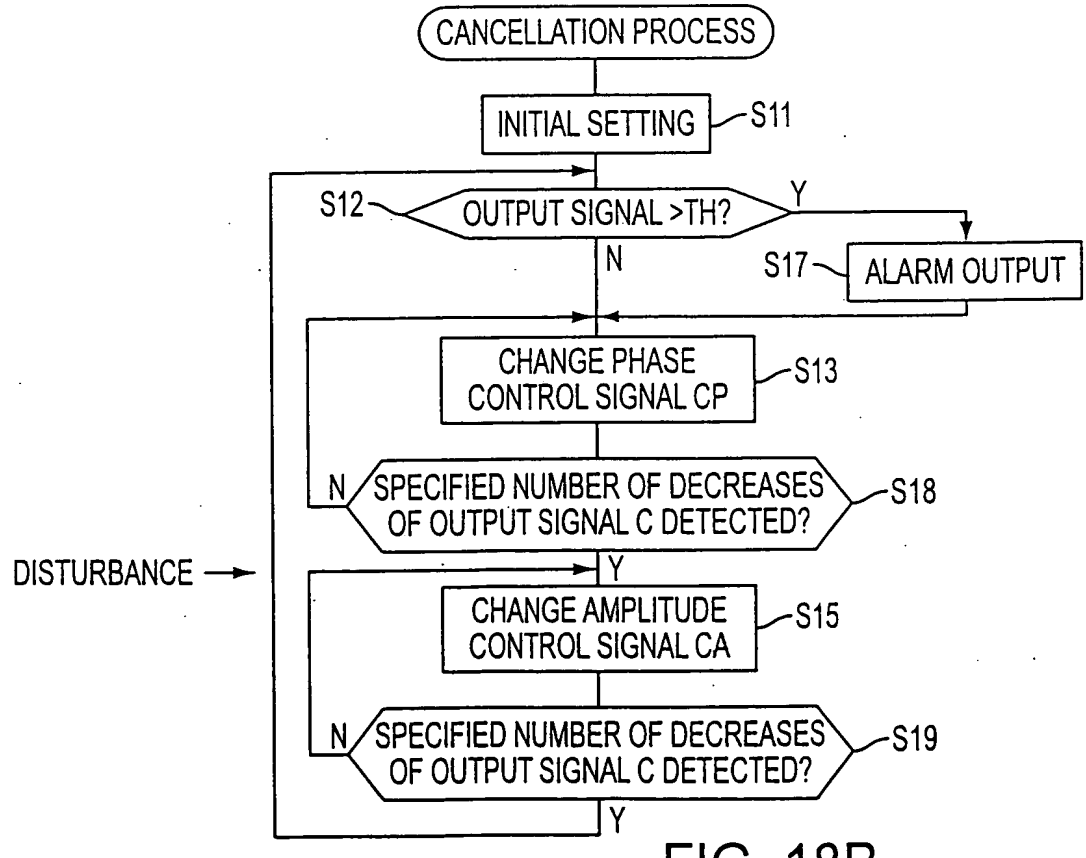


FIG. 18B